An XUP–UNM Educational Platform: A Dual-FPGA Platform for Reconfigurable Logic

C. J. KIEF, MARIOS S. PATTICHIS, L. HOWARD POLLARD, G. ALONZO VERA, JORGE E. PARRA

Department of Electrical and Computer Engineering at the University of New Mexico, Albuquerque, New Mexico 87131

Received 2 September 2007; accepted 3 September 2007

ABSTRACT: We present a new educational platform for teaching reconfigurable logic. The new platform includes two FPGAs, separate instruction and data buses, serial and parallel port connections, and extensive I/O connections for interfacing with other reconfigurable computing boards. The platform was successfully tested at the University of New Mexico, the University of Texas at Austin, the University of Texas at El Paso, and the West Point military academy. Online documentation details the entire design, fabricating, assembly, and testing phases. All design information is freely available online. © 2009 Wiley Periodicals, Inc. Comput Appl Eng Educ 17: 232–239, 2009; Published online in Wiley InterScience (www.interscience.wiley.com); DOI 10.1002/cae.20192

Keywords: FPGAs; education; programmable logic; development board; virtex

INTRODUCTION

Programmable logic popularity among the industry has increased due to its capability to shorten lead-time while also increasing design flexibility. This has led universities to include programmable logic early in their curricula. Even though the use of programmable logic devices in digital electronics labs has been reported as early as 1988 [1,2], new challenges emerge as technology evolves.

There are three fundamental aspects for consideration when teaching programmable logic: pedagogical approaches, software environment, and hardware platforms. We refer the reader to Ref. [3] for a concise summary on reported pedagogical approaches and software environments. We shall argue that in terms of educational hardware platforms there are needs that haven't been fulfilled yet by currently available platforms, which led us to the project described in this article.

Experience using prototyping platforms from different developers (Xilinx, Inc., San Jose, CA,

Correspondence to C. J. Kief (ckief@aegistg.com).

Contract grant sponsor: Xilinx University Program.

C. J. Kief's present address is Aegis Technologies, 6565 Americas Parkway, Suite 825, Albuquerque, NM 87110.

Altera Corporation, San Jose, CA, and Digilent, Inc., Pullman, WA) were reported in Refs. [4−10]. In Ref. [4], the author provides examples for Xilinx and Altera devices. In Refs. [3,5,6], the authors report independent experiences on introducing programmable logic into the first digital lab. In Refs. [3,5], the authors use Xilinx devices. Altera devices are used in Ref. [6]. In all three cases there is no custom development of hardware or software. The labs were implemented with commercially available software, devices, and boards.

In Refs. [7−10], programmable logic is used in advanced digital systems and computer architecture. In Refs. [7,8,10], the authors use both Xilinx and Altera platforms while in Ref. [9], the authors only use an Altera platform. In Ref. [8], a custom peripheral board containing extra memory was designed to work in conjunction with the Xilinx device's board (from Digilent, Inc.).

In all these cases, the commercial or custom boards used contain a single programmable logic device (CPLD or FPGA) for design and prototyping. To the best of our knowledge there is currently no available multi-FPGA platform for programmable logic education. Such a platform would provide a unique starting system for the development of parallel processing systems. In addition, to be useful in a variety of graduate and undergraduate applications, the dual-FPGA platform needs to be inexpensive and robust enough to support a wide-range of projects.

The focus of this article is to describe the development of a comprehensive and stand-alone development environment that provides an inexpensive and robust student-learning platform. Specifically, the objective is to provide a ''roadmap'' that other educational institutions can use to establish a program for the development, fabrication and assembly of a multi-layer PCB platform.

The rest of the article is organized into four sections. Second Section covers the background of programmable logic at UNM and PCB fabrication. Third Section covers the differences between the proposed and the actual system. Fourth Section covers with validation and discussion, and Fifth Section summarizes our conclusions.

BACKGROUND

Programmable Logic at the University of New Mexico (UNM) and PCB Fabrication

Programmable logic was introduced at UNM in 2000. The choice of Xilinx hardware and software as the tools for this paradigm shift was based largely on the extensive series of design tools that were freely available through the Xilinx University Program (XUP). Xilinx's main programmable logic design suite is the Integrated Software Environment (ISE^{TM}). Using this tool, students develop projects using schematic capture, Finite State Machine (FSM), or hardware descriptive language (HDL). During this paradigm shift, UNM realized a need for dual FPGA platforms that were not reasonably affordable through known commercial manufacturers.

Two other development tools that are utilized at UNM include the Embedded Development Kit (EDK) and the System Generator^{TM} (SysGen). EDK allows for development of virtual microprocessors using the Xilinx Microblaze^{TM} system. SysGen is a collaborative effort between Mathworks and the Xilinx Corporation. Mathworks has a tool called Simulink that allows for a graphical design environment. Tutorials associated with these tools are found in Refs. [11−13]. Xilinx developed a series of blocks that are useable within the Simulink design window. The Simulink blocks allow the ability to use traditional Matlab style input sources and plotting options while the Xilinx blocks allow for project development that is directly transferable to the programmable logic. The Xilinx blocks provide for many DSP project capabilities as shown in Ref. [14]. These additional packages greatly benefit from the capabilities delivered through dual FPGAs.

Problem Description, Requirements, and Goals

The overall goal of the project was to develop a high quality, low cost platform that would be cost effective for universities. There are two major categories of users within an academic environment—undergraduate and graduate students. Each of these categories of users have unique requirements that are necessary to ensure a successful learning experience.

Since 2000, the board of choice for UNM student laboratories has been the Digilent series of prototype platforms and plug-in modules. The FPGA and CPLD platforms have proven reliable but they do not make a dual FPGA platform. The XUP−UNM platform was designed to be compatible with the plug-in boards provided by Digilent. As shown in Figure 1, this allows the board to be expanded to include a Liquid Crystal Display (LCD) and seven-segment displays.

As shown in Figure 2, during the design phase, a block diagram of all major components was created. This allowed for a more complete requirements analysis. This diagram was presented to students and

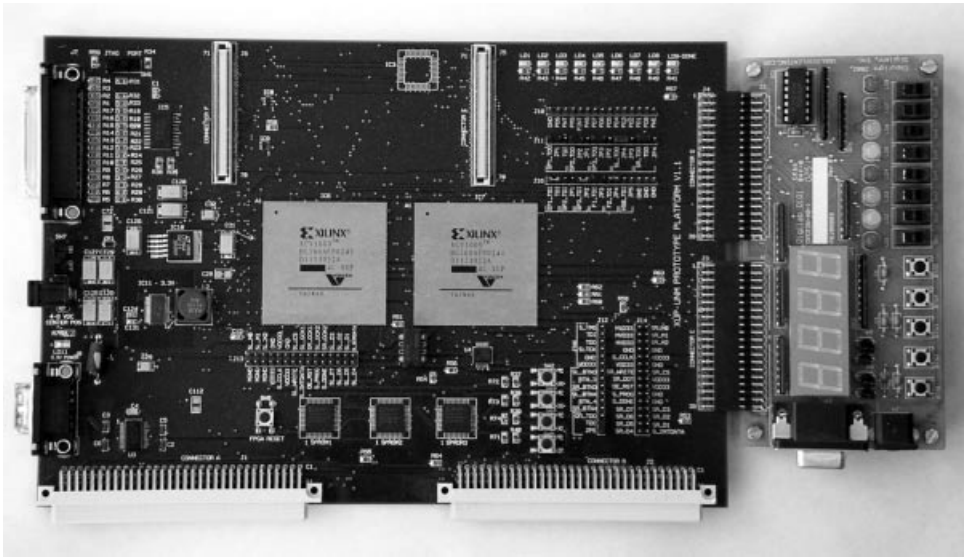

Figure 1 The completed XUP−UNM platform with matted Digilent I/O board is shown here. By co-ordinating the design effort with the Digilent Corporation, interfacing with their series of peripheral input and output boards was accomplished. Their boards possess the capabilities including ADC, DAC, wire wrapping, and LCD.

instructors for feedback to ensure a variety of needs were addressed.

Printed Circuit Board Design

To create the specification document, surveys were taken from 100 different students (undergraduate and graduate). The students indicated that they liked a dual FPGA design, I/O buttons, and LEDs. The online specification document shows what parts were selected and why [15]. The BOM included 275 different parts with the number of parts used, size and temperature characteristics, purchasing sources, and pricing information [16]. Finally, the GBR files were generated using PCB Expedition software. GBR files identify the width and spacing of all runs on the PCB [17].

PROPOSED AND ACTUAL SYSTEM

Overall Board Design

The decision to make the board the selected size and number of layers was made very early in the design process. The smaller the board and less number of layers, the lower the cost. The cost of fabrication is based on physical size of the board (material costs)

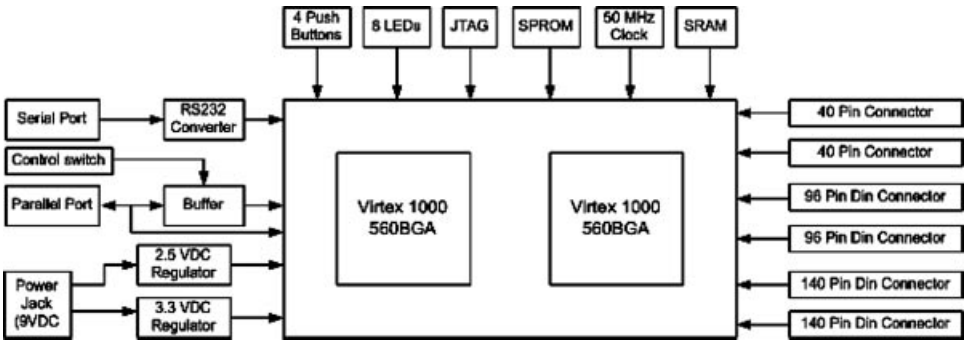

Figure 2 During the design phase, a block diagram of all major components was created. This allowed for a more complete requirements analysis. This diagram was presented to students and instructors for feedback to ensure a variety of needs were addressed.

and on the complexity of lining up layers of boards together. Some parts such as the PowerPad power supply needed an area of isolation around the part for cooling. Since the Ball Grid Array (BGA) devices were the largest and most complicated parts on the platform, they were a leading factor in determining board size, number of layers, and other design considerations. After considering the size of these major sections, eight layers were considered the minimum number of layers possible.

Software Involved

For the board design and layout, development tools manufactured by the Mentor Graphics Corporation were used. For schematic creation, Design Capture software was used, and for PCB development, the Expedition PCB packages were used. The entire design is freely available online. This work can save universities approximately 1-year in design and development time.

FPGA

The Virtex™ V1000s are the main processing components of the XUP−UNM.

Power

The board was designed so that everything that resided on the board could function with only one of two different voltages. The available voltages are 3.3 and 2.5 V. The 2.5 V DC output was developed using a simple voltage regulator that took the 3.3 V DC and converted this input into the desired output. The heart of the voltage section for this project was the Texas Instruments TPS54616 Buck Switching Power Supply. This package can provide a constant 6 Å output for a long period and remain at an acceptable temperature level.

Memory

There are a variety of memories on the XUP−UNM. The board has a footprint for an SRAM chip (not attached). The device of choice was the asynchronous 128 K × 16 Static SRAM from Cypress. To accommodate start-up programming, many designers place memory on the circuit board and connect it through the JTAG chain to allow programming code to the memory and then (upon power cycle) program the FPGA by means of the SPROMs. For this purpose, XC18V00 series SPROMs were chosen [18]. Since the XCV1000 FPGA devices use 6,127,744 configuration bits, each FPGA would require one each XC18V04 and one each XC18V02 PROM solution. To accommodate two of the XCV1000 FPGAs, three each of the XC18V04 devices were used. As shown in Figure 3, this was done by cascading the devices together in a daisy chain configuration.

The master-serial configuration scheme was chosen to provide the capability for programming using the JTAG chain.

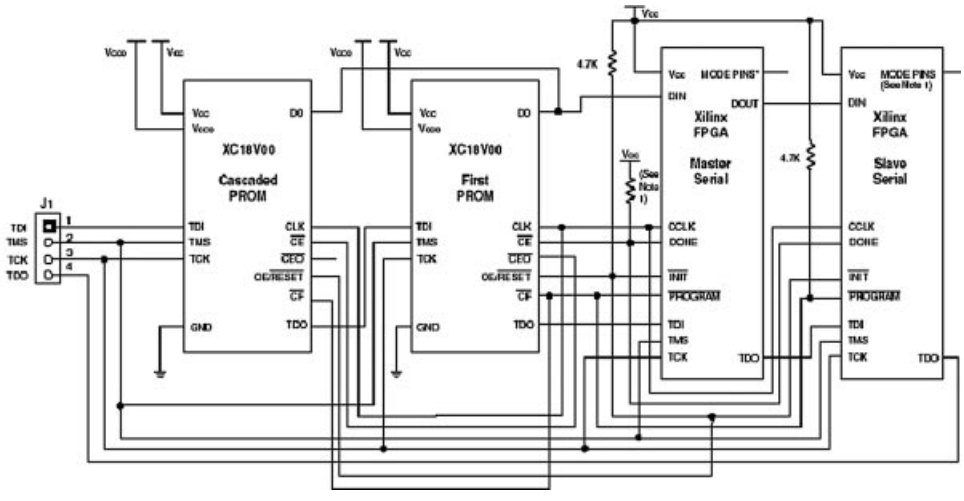

Figure 3 Dual FPGA on a single platform greatly increases the project possibilities available to students. An inexpensive dual FPGA PCB is unavailable from major student platform providers. The interfacing between the cascaded PROMs and the dual FPGA devices was unique and required strict adherence to Xilinx specifications (Courtesy Xilinx Corporation).

VALIDATION AND DISCUSSION

Final Prototype Run

In December 2003, a second set of prototype boards were ordered. Figure 4 shows this final product.

Although minor problems were found, this prototype run was considered solid. This belief is based on feedback from the University of Texas (Austin), the University of Texas (El Paso), West Point Military Academy and its use in UNM classroom environments.

Power Tests

The power system parts were the first items mounted on the board. The process involved mounting several items on the board (using a microscope) and then performing a series of continuity and resistance checks using a Fluke 179 voltmeter. Once all the parts were installed, AC and DC levels were measured over a period of several hours. The FPGA voltages had to be within 5% of the specified 3.3 and 5 V DC values [19]. The voltages measured were 3.301 V DC (from the switching power supply) and 2.504 V DC (from the cascaded voltage regulator). By then measuring the AC ripple, it was possible to determine the level of unwanted noise in the outputs. The output of the switching power supply only had 70 mV of ripple, which was well within the levels of tolerance.

JTAG on the Board

Once all the parts were installed on the platform and verified as having correct signal, power, and continuity connectivity, communication with the board was attempted. There are two ways to communicate with the devices on the XUP−UNM and they both involve the IEEE JTAG chain. The two communications routes go through the 25-pin parallel connector and the six vertical JTAG pins. Both communications routes lead to the same location on the programmable devices. Once a cable is connected between the JTAG pins and a desktop computer, the Xilinx Impact software is used to attempt communications. Using the designed jumpers, it was ensured that each part on the chain could be included, programmed, or excluded.

Signal Testing

The second part of the process was determining that the correct signals were of a level that was acceptable for the rest of the board. Signal testing was performed by several iterations of steps.

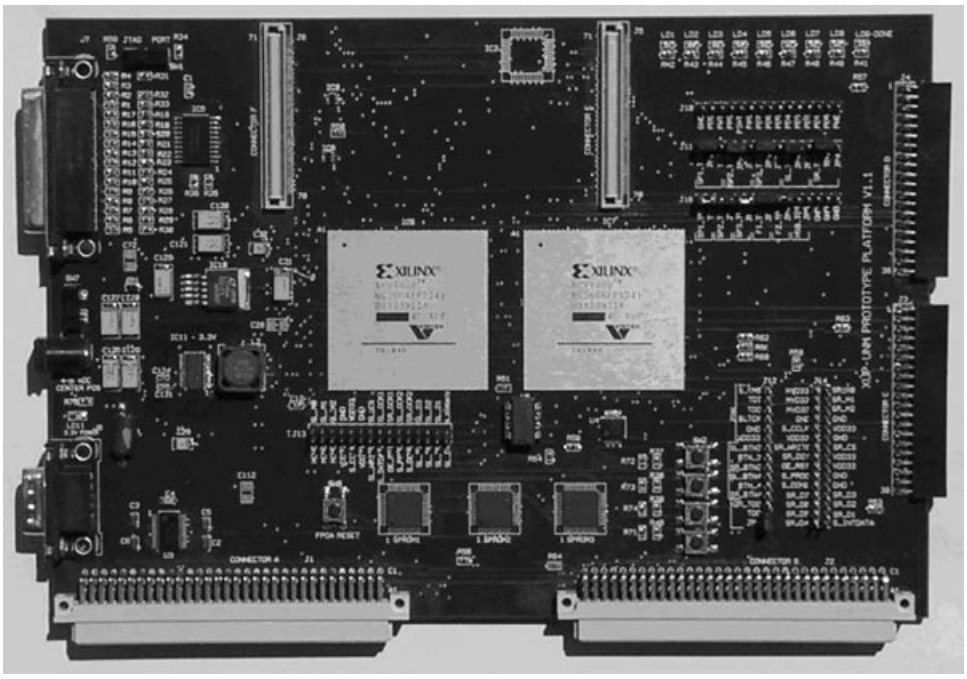

Figure 4 The complete XUP−UNM platform is shown here. This is what was delivered to other universities including West Point and the University of Texas (El Paso) for research and assistance with debugging efforts.

Once it was confirmed that each pin on each connector went to the correct source, power was applied. The next part of the process was ensuring that the correct signals were visible (in terms of quality). To do this, source signals were fed from the FPGAs to the connectors. Using VHDL code, a binary counter was designed to sequentially step through each of the input and output pins on each of the connectors. While they were running, each signal source was then verified using an oscilloscope.

Serial Testing Using EDK

To verify the functional operation of the serial section, a project was developed using the EDK software. As shown in Figure 5, this software used a virtual microprocessor to print ''Go Lobos'' to a HyperTerminal.

This test allowed for checking out the entire serial path from the FPGA to the output of the 9-pin serial connector.

Educational Impact

The impact of this project spans a wide-range of organizations from academia to industry. Some of the academic organizations that were directly impacted by this project were the University of Texas (Austin), the University of Texas (El Paso), the West Point Military Academy, and the University of New Mexico. From our phone and email conversations with the participating Universities, we have verified that they were able to duplicate basic board tests, as we describe in the previous sections.

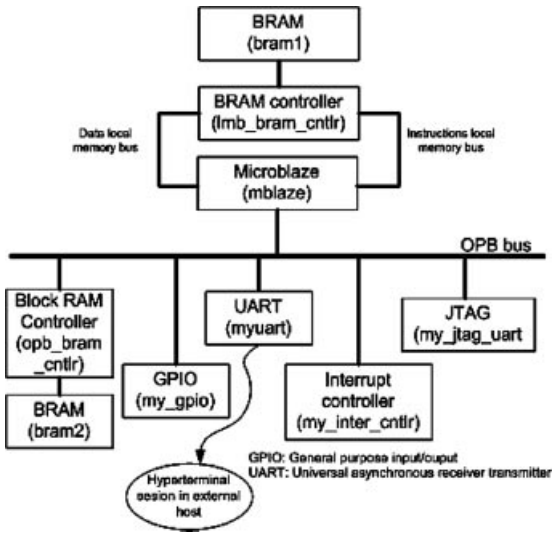

Figure 5 Part of the testing phase included developing projects to use on the board (and to provide to other universities). This project (freely available online) is a virtual Microblaze microprocessor that was used to drive a HyperTerminal and an LED.

The greatest impact has been on the Department of Electrical and Computer Engineering at the University of New Mexico. This prototype platform allowed ECE to begin teaching aspects in Computer Engineering that were not possible before. This new platform was affordable enough to allow its introduction into the Senior Design Laboratory course curriculum. This introduction allowed projects to be completed that were not possible before due to limited numbers of input−output pins and single FPGA commercial platforms. The project led to four senior design projects, a Masters thesis, and significant experience in parallel reconfigurable computing architectures for two PhD students and two Professors (Prof. Pattichis and Prof. Pollard).

The involvement with the local Xilinx Corporation allows us to build a stronger relationship that resulted in UNM being able to provide them with a source of employees for their multinational corporation that had not only basic engineering knowledge but also actual hands on skills in the board development arena.

Ultimately, the expertise gained by the authors led to their involvements in the establishment of the FPGA mission assurance center (FMAC) at the University of New Mexico (see www.fpgamac.com). FMAC is a New-Mexico consortium that includes the Air-Force Research Laboratory, the University of New Mexico, Sandia National Laboratory, the Los Alamos National Laboratory, and Xilinx.

Similarly, the successful testing of the board at other Universities provided strong encouragement for enhancing their curricula in reconfigurable computing. According to Colonel Bryan Goda, an academy instructor at West Point, ''This board has great potential within an undergraduate curriculum. We are looking forward to seeing what it can do.'' Training sessions for the boards were provided for all off-site locations. Thus, for the schools outside of New Mexico, it is believed that the efforts of the XUP−UNM and the individuals involved may have helped to ''jumpstart'' the programmable logic programs at those schools. By providing them with complete instructional labs, guidance, tutorials and a platform to develop them on, they were able to move forward in their programs. At the University of Texas at Austin, the second course in Digital Systems design has been renamed to include VHDL. This course is

now called: "EE 360M: Digital Systems Design Using VHDL." Similarly, the University of Texas at El Paso is now offering: "EE 3109 Computer Aided Digital Design."

CONCLUSIONS

We have presented a new board for reconfigurable computing education that provides a paradigm of interconnecting two FPGAs with serial and parallel connections and daughter board interface. An advanced design of the JTAG chain allows for inclusion or exclusion of all programmable logic devices on the board for project development. Several undergraduate and three graduate students participated in the development of the board. A number of Universities participated in testing the boards. At the University of New Mexico, the experience gained by the board design led to the development of a more advanced board and the establishment of the FPGA mission assurance center (FMAC). All documentation associated with the board is available online and can be used as a starting point for the design of new boards that can greatly benefit from the component interface examples.

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BIOGRAPHIES

Craig Kief is a senior systems engineer at AEgis Technologies Group and is currently serving as the deputy director of the FPGA Mission Assurance Center (FMAC). He is a member of a development team creating a laser scene generator under contract for the Air Force Research Laboratory. Craig has published numerous articles and taught courses in the area of programmable logic and Verification, Validation, and Accreditation of systems. He has a Masters Degree in Computer Engineering from the University of New Mexico. He is a certified modeling and simulation professional through M&SPCC and can be reached at asstdirector@fpgamac.com.

Dr. Marios S. Pattichis received the BSc (high honors and special honors) in Computer Sciences in 1991, the BA (high honors) in Mathematics in 1991, the Master of Science in Engineering in 1993, and the PhD in computer engineering in 1998, all from the University of Texas at Austin. He is currently an associate professor with the Department of Electrical and Computer Engineering at the University of New Mexico (UNM), Albuquerque, New Mexico. At UNM, he received the 2004 ECE distinguished teaching award and the 2006 School of Engineering Harrison faculty recognition award.

Dr. Howard Pollard is an assistant professor with the Department of Electrical and Computer Engineering at the University of New Mexico. He has taught courses in Digital Design, Advanced Digital Design, Design of Computers, Microprocessors, Computer Architecture, Hardware Design with VHDL, and Embedded System Design. He has designed or managed the design of complex digital systems both in general purpose processors and high-speed programmable logic systems. He has authored two books on computer architecture. He holds BS and MS degrees in electrical engineering from Utah State University and a PhD from the University of Illinois, also in electrical engineering.

G. Alonzo Vera received the BSc in electrical engineering in 1998 from the Pontificia Universidad Catolica del Perú, Lima, Perú, and the MSc in electrical engineering in 2004 from the University of New Mexico. He is currently a PhD Candidate with the Department of Electrical and Computer Engineering at the University of New Mexico (UNM), Albuquerque, New Mexico. His research interests include reconfigurable computing and digital signal processing.

Jorge Parra received the BSc degree in electronics engineering from Pontificia Universidad Javeriana, Bogotá, Colombia in 1999. He received his MSc in electrical engineering with a concentration in computer engineering from the University of New Mexico in 2004. Currently he is a PhD candidate in the Electrical and Computer Engineering Department at the University of New Mexico. His research interests include Computer Architecture and Design, Digital Design and Artificial Intelligence.